A HISTORY OF INDUSTRY INNOVATION— ULTRAFLAT POLISHED SILICON WAFERS

Early Challenges for Flatter Wafers

In the early to mid 1960s, the Department of Defense began pushing the infant semiconductor industry with a desire to replace the vacuum tubes in the Minuteman ballistic missiles with solid state integrated circuits. The impetus by the Defense Department caused an even greater interest and demand by semiconductor device makers for flatter silicon wafers. While epi technology was still in development in MEMC and in the silicon industry, MEMC also began to invest resources to produce ultraflat silicon wafers.

In 1961 Bob Walsh came to Monsanto Silicon Research from the corporate Central Research Department in Dayton where he had developed growing processes for Gallium Arsenide. The big challenge was to create flat, damage-free surfaces for depositing an epi layer on silicon wafers. The only way to polish in those days was to use abrasives that left too much damage on the wafer. At this time, MEMC was selling lapped slices, and the customer etched them to remove damage before they built discrete transistor and rectifier devices. The problem was that etching did not produce the smooth mirror surface needed for high resolution photolithography.

MEMC Pioneers Revolutionary Polishing Techniques

In 1962 MEMC began to work on new polishing techniques to obtain a smoother and flatter surface on which to build more advanced devices. Wafers were about 5/8 inch diameter at this time!

MEMC's team under Walsh developed the idea of using colloidal silica, then made by Monsanto, for the polishing agent instead of the usual abrasives. This polishing technique eliminated residual surface damage which allowed the deposition of high quality epi layers. This was the birth of what is now known as chemical-mechanical polishing, still the standard used worldwide for polishing silicon wafers. This method works because the surface layers are removed by chemical action while the surface flatness is generated by the mechanical action of the polisher.

In the 1965-1966 time frame, there was also a great deal of work done to improve the thickness variation of polished wafers. This research resulted in the development of the "spin" mounting process, which many in the industry still use today to generate very uniform layers of wax for mounting wafers on the polishing blocks. During the late 60's a free mounting process was developed that did not require wax. This allowed simplified process flow since the polishing blocks did not have to leave the polishers for mounting.

MEMC Innovates Automated Polishing Processes

In the mid 70's, flatness was again becoming an issue with the customers and Monsanto wafers made on the free mount process were the flattest wafers in the market. Perkin Elmer, who made optical steppers, used Monsanto wafers to calibrate their instruments. During this time, Canon, Siltec, and ADE began to make measurement equipment for determining flatness on silicon wafers.

By the late 70's, an improved automated polishing process was developed. The machine, called the Mark 8 polisher, used wax mounting and a machine design conceived by Harold Hileman and built by Strasbaugh. In 1978, MEMC's St. Peters plant began using this process to polish wafers on the world's first automated wax mount polishing line. In 1981, the machine was enlarged to improve performance on large wafers. The new polisher was called the Mark 8A.

In the early 1990's, MEMC was developing 150mm and 200mm single wafer polishing processes. These processes utilized the new Mark 9K polisher, again conceived by H. Hileman and developed by MEMC and Strasbaugh. Part of this project was the successful development of an environmentally-friendly mounting wax called "green wax," which does not require chlorinated hydrocarbon solvents. The Mark 9K polisher was the first "cassette to cassette" automated wafer polisher to fully integrate all wafer mounting, polishing, and demounting functions into a single machine. Because of the tight control over all process steps, this machine is capable of producing exceptionally flat 200mm wafers.

Meeting the Flatness Challenges Today

Today, silicon wafer flatness is a critical parameter that affects many aspects of semiconductor fabrication including microlithography. While device makers are continually shrinking line widths and tool makers are becoming more and more precise, the surface nanotopography of the silicon wafer becomes more and more important. MEMC is working on improvements in polishing and wafer flatness using both single-sided and double-sided polishers. MEMC's history demonstrates that we have been committed in the past to pioneering innovation and developing industry standards with tool makers for polishing and wafer flatness. MEMC's current research demonstrates that it will continue to be committed to providing customers with the very flattest wafers possible.